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# A hardware/software co-simulation environment for micro design with HDL simulator and OS interface

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**Abstract**
Proposes a hardware/software co-simulation environment using an RTL (register transfer a software language interface. The proposed simulation environment introduces the "oper interface" (OSIF), which invokes system calls in the OS on the simulation platform to exec software. The OSIF consists of data adaption facility and function correspondence manag cooperate with the OS of the simulation platform. We show the results of experiments with compatible processor model. This environment verified our processor model with SPEC b require various OS services. For example, with the Lisp interpreter program li, our detailec the core part of R3000 was simulated only within 20 hours on a 109 MIPS workstation

**Index Terms**
**Inspec**
**Controlled Indexing**
LISP application program interfaces hardware description languages logic CA microprocessor chips operating systems (computers) performance evaluation interpreters virtual machines

**Non-controlled Indexing**
109 MIPS 20 hour HDL simulator Lisp interpreter OSIF R3000-compatible p model RTL simulator SPEC benchmarks application software data adaption f function correspondence management hardware description language simulator hardware/software cosimulation environment li interpreter program microproces operating system interface register transfer level simulator simulation platform language interface system call invocation workstation

**Author Keywords**
Not Available

**References**

No references available on IEEE Xplore.

**Citing Documents**

No citing documents available on IEEE Xplore.